The Flash System 900 and IBM Power Node S822LC

At the UMBC’s CHMPR, a future state-of-the-art Accelerated Cognitive Computer System (ACCS) for Big Data science is being integrated into the current IBM iDataplex computational system ‘bluewave’.

Based on the next gen IBM 200 Petaflops summit processor, an interim 2 nodes of IBM Power S822LC testbed is being integrated with dual Power 8+ processors with 10 cores at 3.0 GHz and four Nvidia Tesla P100 GPUs with 2 Nvidia's NVLinks from the power 8+ to each pair of GPUs, keeping the data moving fast between them.

We also have the Flash system 900 with 30TB of flash ram expandable to 40 TB connected to the S822LC nodes with a Coherent Accelerator Processor Interface (CAPI) fpga and an additional NVME card with 8TB of SSD. The flash ram system supports both nodes and the storage partitioning. The flash ram allocation is programmable.
ADDITIONAL INFORMATION ABOUT THE IBM S822LC POWER NODES

PROCESSOR AND MEMORY

MICROPROCESSORS: ONE 10-CORE 2.92 GHZ POWER8 PROCESSOR CARD
LEVEL 2 (L2) CACHE: 512 KB L2 CACHE PER CORE
LEVEL 3 (L3) CACHE: 8 MB L3 CACHE PER CORE

MEMORY: 1 TB

PROCESSOR-TO-MEMORY BANDWIDTH: 115 GB/SEC

STORAGE AND INPUT/OUTPUT (I/O)

STANDARD BACKPLANE: STANDARD MEZZANINE CARD SUPPORTS TWO LFF BAYS IN REAR
12 LFF BAYS IN FRONT REQUIRE A DISCRETE RAID ADAPTER TO ENABLE

RAID OPTION: HW RAID COMES FROM OPTIONAL PCIE ADAPTER
FOUR PCIE GEN3 ADAPTER SLOTS:

3XPCIE X8, 1 IS CAPI ENABLED
1XPCIE X16, CAPI ENABLED

I/O BANDWIDTH: 32 GB/SEC

POWER SUPPLY: 100 V TO 240 V

RAS FEATURES:

PROCESSOR INSTRUCTION RETRY
SELECTIVE DYNAMIC FIRMWARE UPDATES
CHIP KILL MEMORY
ECC L2 CACHE, L3 CACHE
SERVICE PROCESSOR WITH FAULT MONITORING
HOT-SWAPPABLE FRONT DISK BAYS
HOT-PLUG AND REDUNDANT POWER SUPPLIES
REDUNDANT COOLING FANS

OPERATING SYSTEM: UBUNTU LINUX ON POWER
SYSTEM DIMENSIONS: 450 W X 87 H X 711 D MM